IN THE CLAIMS:

1. (Currently Amended) A chip carrier comprising:

a base having a surface and a periphery;

an inner well having a periphery extending along the periphery of the base and wherein the inner well has a second base having a second depth between the second base and the surface;

an outer well extending along the periphery of the inner well, and wherein the outer well has a first base having a first depth between the first base and the surface, wherein the first depth is greater than the second depth.

2. (Currently Amended) The chip carrier according to claim wherein the ~~first~~ inner well and the ~~second~~ outer well form a flexible structure.

3. (Original) The chip carrier according to claim 1 wherein the outer well includes an outer wall and an inner wall and the inner well includes an outer wall coupled to the inner wall of the outer well.

Kindly cancel Claim 4 without prejudice or disclaimer

5. (Previously Presented) The chip carrier according to claim 1 further comprising an integrated circuit removably positioned on the base.

Claim 6-20 (Canceled)

21. (Previously Presented) The chip carrier according to claim 1 further comprising:

an upper surface;

an integrated circuit positioned on the base and below the upper surface, the integrated circuit having leads;

wherein the inner well has a base, the leads positioned above the base and below the upper surface.

22. (Previously Presented) The chip carrier according to claim 1 wherein the base, the inner well, and the outer well form an integrated circuit carrier and the chip carrier further comprises a plurality of integrated circuit carriers.

23. (Previously Presented) The chip carrier according to claim 1 further comprising a cover adapted to hold an integrated circuit in the chip carrier.

24. (Previously Presented) The chip carrier according to claim 1 further comprising a cover for holding an integrated circuit in the chip carrier.

25. (Currently Amended) A chip carrier comprising:

a base having a surface and a periphery;

an inner well having a periphery extending along the periphery of the base and wherein

the inner well has a second base having a second depth between the second base and the surface;

an outer well extending along the periphery of the inner well, and wherein the outer well has a first base having a first depth between the first base and the surface, wherein the first depth is greater than the second depth; and

the chip carrier adapted to temporarily hold an integrated circuit in the chip carrier.

26. (Previously Presented) The chip carrier according to claim 25 wherein the base, the inner well, and the outer well form an integrated circuit carrier and the chip carrier further comprises a plurality of integrated circuit carriers.

27. (Previously Presented) The chip carrier according to claim 25 further comprising a cover adapted to hold an integrated circuit in the chip carrier.

28. (Previously Presented) The chip carrier according to claim 25 further comprising a cover for holding an integrated circuit in the chip carrier.

29. (New Claim) The chip carrier according to claim 1 wherein the first depth is about 1.219 mm and the second depth is about .869 mm.

30. (New Claim) The chip carrier according to claim 1 wherein at least one of the outer well or the inner well encircle the base.

31. (New Claim) The chip carrier according to claim 1 further comprising an upper surface and wherein the outer well extends farther away from the upper surface than the inner wall.

32. (New Claim) The chip carrier according to claim 31 wherein the outer well extends about 2.716 mm away from the upper surface and the inner well extends about 2.366 mm away from the upper surface.